REMARKS

As a preliminary matter, Figure 1 is now designated as "Prior Art". Accordingly, Applicants request withdrawal of the objection to the drawings.

As a further preliminary matter, the title of the invention is amended to "Data Processing Device for Processing Data Accessed by a Buffer Manager, and Interface Device." Withdrawal of the objection to the title is respectfully requested.

Claims 1-3 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kozakai et al. (U.S. Patent No. 6,643,725). Applicants respectfully traverse the rejection because the cited reference does not disclose (or suggest) a data processing device that has the processor, buffer manager, and shared memory interconnected by an internal bus, which decreases the processing time needed to read or write data in the shared memory.

Kozakai is directed to a memory card having a buffer memory for storing and testing instructions. The memory card has the execution of instructions by a data processor controlled in response to external commands. The program executed by the central processing unit (CPU) 30 of the data processor 3 is changed according to a command from a host interface 11 of an interface control circuit 2. When a command CMD 1 is received, a program PG1 stored in buffer RAM 7 is executed. Similarly, when a command CMD 2 or CMD 3 is received, a program PGM 2 or PGM 3 stored in integrated ROM 34 is executed. The buffer RAM 7 is mapped to an address space of the CPU 30. The CPU 30 or the microcomputer 3 can access the buffer RAM 7 in a similar manner to access the work RAM

8 through the data transfer logic 14. The buffer RAM 7 functions as a data buffer when transferring data to or from a flash memory 4. The buffer RAM 7 also functions as a data buffer when transferring data from the flash memory forward to the work RAM 8 and vice versa.

However, Kozakai teaches to take the data transfer path of the data processor 3, the interface control circuit 2, and the buffer RAM (SRAM) 7 in this order. Kozakai fails to teach (or suggest) having the processor (CPU), the buffer manager and the shared memory (SRAM) interconnected by an internal bus, as in the present invention.

That is, the data processing device of the present invention has the processor (CPU), the buffer manager and the shared memory (SRAM) interconnected by an internal bus. Accordingly, the processing time needed to read or write data in shared memory can be shortened. Since Kozakai relies on external commands to control execution of instructions by the data processor, and does not have the processor, buffer manager, and shared memory interconnected, as in the present invention, withdrawal of the §102(e) rejection is respectfully requested.

Claims 9-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kozakai. Applicants respectfully traverse the rejection because Kozakai fails to teach or suggest a processor, interface device and first and second buffer memories that are interconnected, as in the present invention.

As noted above, the present invention has the processor, the interface device

and the buffer memories interconnected by an internal bus. This improves processing time for reading or writing data in each buffer memory. Since Kozakai does not disclose or suggest this feature of the present invention, for at least this reason, withdrawal of the §103 rejection is respectfully requested.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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